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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,114	11/05/2001	Hung T. Nguyen	01-633	6984

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,114	NGUYEN ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER 5/1/2006
GROUP 2100
AU 2181

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Henry et al., US Patent 6,421,774 (Herein referred to as Henry). The rejections as set forth in the last office action mailed on October 5, 2005 are respectfully maintained and included below.

4. Referring to claim 1, Henry has taught for use in a wide-issue processor, a mechanism for conditionally executing instructions, comprising:

a. a conditional execution block state machine that tags and generates link pointers for instructions located in a conditional execution block (Figure 1, Instruction pointers, column 6, line 62-column 7, line 44); and

b. conditional link pointer register sets (Figure 1, elements 134, 144, 136, 146, 138, 148, 130, and 140), wherein each of said sets corresponds to a stage of a pipeline of said processor (Figure 1, elements 134 and 144 correspond to the register stage, elements 136 and 146 correspond to the address stage, elements 138 and 148 correspond to the data stage, and elements 130, and 140 correspond to the write back stage.), that contain and cause said link pointers to move through each of said sets as said instructions associated with said link pointers and located in said conditional execution block move through stages (Figure 1, column 7, lines 25-59, elements 134, 144, 136, 146, 138, 148, 130, and 140).

5. Referring to claim 2, Henry has taught the mechanism as recited in Claim 1, as described above, and further comprising a conditional execution marking queue, associated with said conditional execution block state machine, that contains ones of said link pointers prior to storage in said sets (Figure 1, Elements 151, 142, and 103 comprise the claimed execution marking queue.).

6. Referring to claim 3, Henry has taught the mechanism as recited in Claim 2, as described above, and wherein said conditional execution marking queue is a five-bit, six-entry queue (Figures 1, 3, and 4, column 10, lines 38-45, At least 12 bits, or entries, are in the queue.) and comprises a reordering multiplexer (Figure 1, element 151).

7. Referring to claim 4, Henry has taught the mechanism as recited in Claim 1, as described above, and further comprising a conditional execution attribute register, associated with a group stage of said pipeline, that contains an attribute associated with one of said conditional instructions (column 2, lines 34-61, column 5, line 20-column 6, line 28, element 103, The

branch history bits for instructions are stored in a conditional execution attribute register of the history table in the branch predictor, element 103).

8. Referring to claim 5, Henry has taught the mechanism as recited in Claim 1, as described above, and where said conditional execution block state machine generates said link pointers that mark the beginning and end of a conditional execution block of instructions (Column 10, lines 11-23, Instruction pointers that point to a taken branch target address mark the beginning of a conditional execution block of instructions. On a branch taken misprediction, the instruction pointer marks the end of the conditional execution block of instructions by pointing to the next sequential instruction.).

9. Referring to claim 6, Henry has taught the mechanism as recited in Claim 4, as described above, and further comprising a conditional execution attribute queue that contains attributes read from said conditional execution attribute register (Figure 1, elements 103, 134 136, 138, and 130 comprise the conditional execution attribute queue.).

10. Referring to claim 7, Henry has taught the mechanism as recited in Claim 6, as described above, and wherein said conditional execution attribute queue is of variable depth (column 10, lines 38-44, column 11, lines 21-29) and comprises a selecting multiplexer (Figure 1, element 103, Figure 4, element 414).

11. Claims 8 and 15 do not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

12. Claims 9 and 16 do not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

13. Claims 10 and 17 do not recite limitations above the claimed invention set forth in claim 3 and is therefore rejected for the same reasons set forth in the rejection of claim 3 above.

14. Claims 11 and 18 do not recite limitations above the claimed invention set forth in claim 4 and is therefore rejected for the same reasons set forth in the rejection of claim 4 above.

15. Claims 12 and 19 do not recite limitations above the claimed invention set forth in claim 5 and is therefore rejected for the same reasons set forth in the rejection of claim 5 above.

16. Claims 13 and 20 do not recite limitations above the claimed invention set forth in claim 6 and is therefore rejected for the same reasons set forth in the rejection of claim 6 above.

17. Claims 14 and 21 do not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

Response to Arguments

18. Applicant's arguments filed January 9, 2006 with respect to claims 1-21 have been fully considered but they are not persuasive.

19. On page 3, Applicant argues in essence:

"The Examiner asserts that the instruction pointers of Henry disclose the link pointers that are generated for instructions located in a conditional execution block, as recited in independent claims 1, 8 and 15. The instruction pointers are not generated for instructions located in a conditional execution block but instead are target addresses that the fetcher 101 uses to fetch instructions. (See column 6, lines 62-64.) The Applicants do not find where Henry even discloses a conditional execution block, or more specifically generating a link pointer for instructions that are in conditional execution block. The instruction pointers, therefore, do not teach the link pointers that are generated for

instruction located in a conditional execution block as recited in independent Claims 1, 8, and 15."

However, the instruction pointer of Henry points to a possible target of a conditional branch instruction. Branch target instructions that follow a conditional branch instruction are the claimed conditional execution block. The conditional execution block gets executed, or not, depending on an opcode of an instruction preceding the conditional branch instruction, therefore the branch instruction is conditional. So Henry has in fact taught link pointers that are generated for instructions located in a conditional execution block (Figure 1, Instruction pointers, column 6, line 62-column 7, line 44, Instruction pointers for conditional branch instructions are generated for branch target instructions following a conditional branch instruction (i.e. for a conditional execution block), based on an opcode of an instruction preceding the conditional branch instruction. The link pointers are saved in elements 142, 144, 146, 148 and 140.). Therefore this argument is moot.

20. On pages 3-4, Applicant argues in essence:

"Additionally, even assuming that the instruction pointers are link pointers, the IP's (144, 146, 148 and 140) and the static prediction registers (134, 136, 138 and 130) are not conditional link pointer register sets as asserted by the Examiner. Instead, each of the IPs is a single register wherein a branch instruction address is piped down and each of the static prediction register is a single register wherein static prediction information is piped down."

However, Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11,15 (CCPA 1978).

> *"It is the claims that measure the invention." SRI Int'l v. Matshshita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).*
>
> *"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." In re Hiniker Co., 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).*
>
> *"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." In re Morris, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).*
>
> *"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." Intervet Am., v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).*
>
> *"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." In re Paulsen, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).*

In the case of claim 1, Applicant has merely claimed *"conditional link pointer register sets, wherein each of said sets corresponds to a stage of a pipeline of said processor, that contain and cause said link pointers to move through each of said sets as said instructions associated with said link pointers and located in said*

conditional execution block move through each of said corresponding stages." In Henry, Figure 1, elements 134 and 144 correspond to the register stage conditional link pointer register set, elements 136 and 146 correspond to the address stage conditional link pointer register set, elements 138 and 148 correspond to the data stage conditional link pointer register set, and elements 130, and 140 correspond to the write back stage conditional link pointer register set. Each register set corresponds to a stage of the pipeline of the processor. The link pointers move through the register sets in elements 142, 144, 146, 148 and 140 as the instructions move through the stages. It is noted that Applicant has not claimed that link pointers move through each register of each register set as instructions move through the stages. Therefore this argument is moot.

Conclusion

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

22. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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5/1/2006